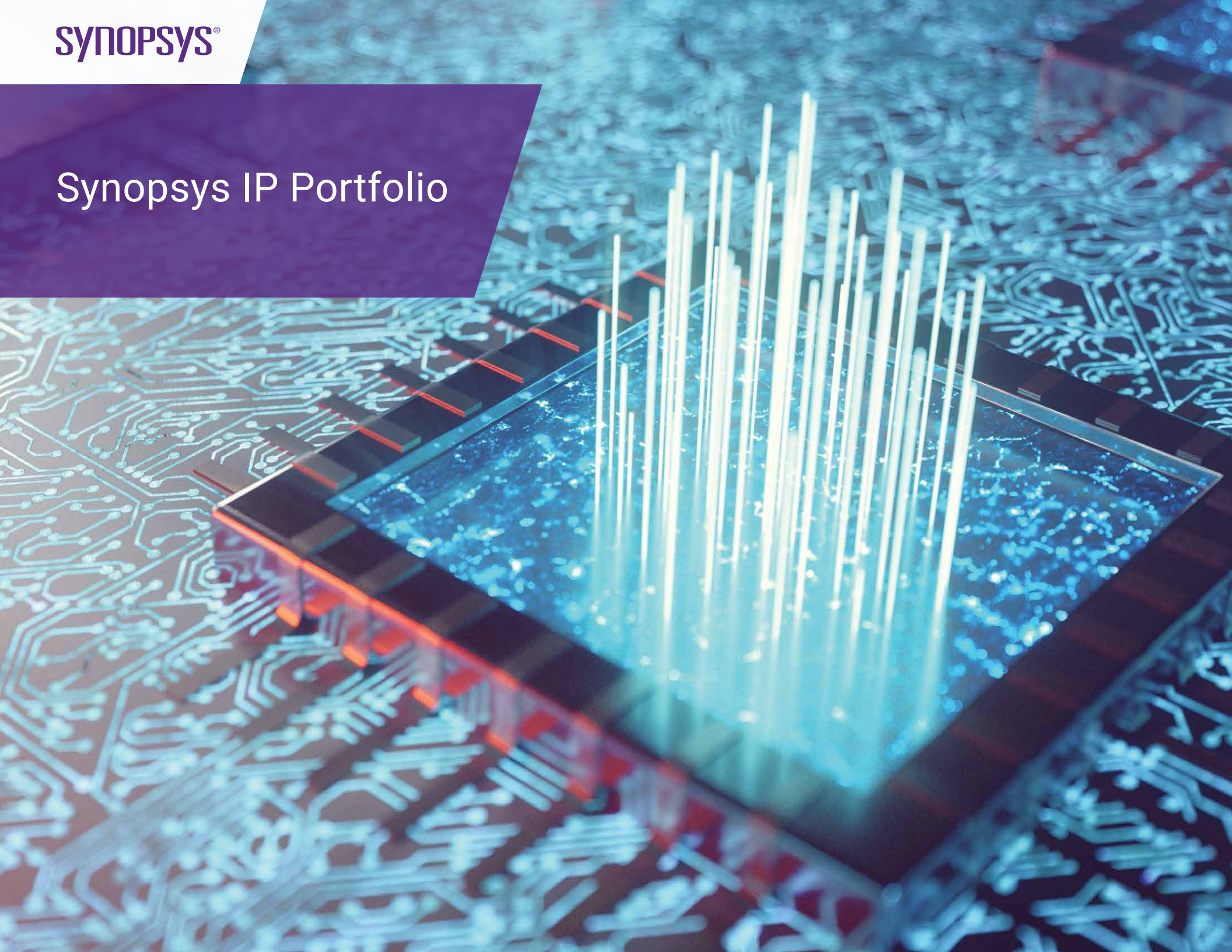
SYNOPSYS®

Synopsys IP Portfolio



Broad IP Portfolio

Synopsys is a leading provider of high-quality, silicon-proven semiconductor IP solutions for SoC designs. The broad Synopsys IP portfolio includes logic libraries, embedded memories, interface IP, security IP, embedded processors and subsystems. To accelerate IP integration, software development, and silicon bring-up, Synopsys' IP Accelerated initiative provides architecture design expertise, pre-verified and customizable IP subsystems, hardening, and signal/power integrity analysis. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enables designers to reduce integration risk and accelerate time-to-market.

Interface IP													
Die-to-Die	Process Technologies							Controllers	Supported Protocol				Verification IP
	16nm	12nm	7nm	6nm	5nm	4nm	3nm		Streaming	CXS	CHI-C2C	CXL	
UCIe					✓	✓	✓	✓	✓	✓	✓	✓	✓
HBI/AIB	✓		✓		✓								
112G XSR		✓	✓	✓	✓			✓		✓			

PCI Express	Process Technologies									Controllers	Configuration	IDE Security Module	HS Access & Test	Verification IP	Auto Grade
	40/45/55/65nm	28nm	22nm	20nm	12/14/16nm	8/10nm	7nm	5/6nm	3/4nm						
PCIe 7.0								✓	✓	Endpoint, Root Port, Dual Mode, Switch	x2, x4, x8	✓	✓	✓	
PCIe 6.x								✓	✓	Endpoint, Root Port, Dual Mode, Switch	x2, x4, x8, x16	✓	✓	✓	
PCIe 5.0					✓	✓	✓	✓	✓	Endpoint, Root Port, Dual Mode, Switch, Embedded Endpoint	x1, x2, x4, x8, x16	✓	✓	✓	✓
PCIe 4.0		✓			✓		✓	✓	✓	Endpoint, Root Port, Dual Mode, Switch, Embedded Endpoint	x1, x2, x4, x8, x16	✓	✓	✓	✓
PCIe 3.1		✓	✓		✓	✓	✓	✓	✓	Endpoint, Root Port, Dual Mode, Switch, Embedded Endpoint	x1, x2, x4, x8, x16	✓	✓	✓	✓
PCIe 2.1	✓	✓	✓	✓	✓		✓	✓	✓	Endpoint, Root Port, Dual Mode, Switch, Embedded Endpoint	x1, x2, x4, x8, x16		✓	✓	✓

Interface IP										
Ethernet	Process Technologies					PCS	Controllers	MACSec	Verification IP	Auto Grade
	28nm	14/16nm	7nm	5nm	3nm					
224G Ethernet (200G/400G/800G/1.6T)					✓	✓	✓		✓	
112G Ethernet (100G/200G/400G/800G)			✓	✓	✓	✓	✓	100G	✓	
56G Ethernet (100G/200G/400G)		✓	✓	✓	✓	✓	✓	100G	✓	
RXAUI/Double XAUI (6.25 G)	✓	✓	✓	✓	✓	✓	✓	✓	✓	
1000BASE-KX, 10GBASE-KR, 10GBASE-KX4	✓	✓	✓	✓	✓	✓	✓	✓	✓	
40GBASE-KR4, 40GBASE-CR4, XLAUI	✓	✓	✓	✓	✓	✓	✓	✓	✓	
100GBASE-CR10, CAUI	✓	✓	✓	✓	✓		✓	✓	✓	
100GBASE-DR4/CR4, CAUI4							✓	✓	✓	
100GBASE-KR2/1		✓	✓	✓	✓		✓	✓	✓	
SGMII	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
QSGMII	✓	✓	✓	✓	✓	✓	✓	✓	✓	
XFI, SFI (SFF-8431)	✓	✓	✓	✓	✓	✓	✓	✓	✓	
GMII/MII, RGMII, RTBI, TBI, SMII, RMII, RevMII, XGMII, XLGMII						✓	✓	✓	✓	
IEEE TSN/AVB Standards: IEEE 802.1AS, 802.1AS-Rev, 802.1Qav, 802.1Qat, 802.1Qbv, 802.1Qbu & 802.3br							✓	✓	✓	✓
25G/50G Ethernet Consortium and IEEE specifications		✓	✓	✓	✓	✓	✓	✓	✓	
2.5G/5.0G USXGMII		✓	✓	✓	✓	✓	✓	✓	✓	
Additional Enterprise Protocols										
OIF, CEI-6G/11G	✓	✓	✓	✓						
CPRI, OBSI, JESD204 A/B	✓	✓	✓	✓					✓	
SRIO	✓	✓	✓	✓						

Interface IP

HBM	Process Technologies				Controllers	Platform Architect Support	Verification IP
	7nm	6nm	5nm	3nm			
HBM3E	✓	✓	✓	✓	✓	✓	✓
HBM2E	✓	✓	✓				✓

DDR	Process Technologies									Controllers	Inline Memory Encryption (IME) Security Module	Platform Architect Support	Verification IP	Auto Grade
	40/45nm	28nm	22nm	14/16nm	12nm	10nm	7nm	5nm	3nm					
LPDDR5X				✓	✓		✓	✓	✓	Memory controller	✓	✓	✓	✓
LPDDR5				✓	✓		✓	✓	✓	Memory controller	✓	✓	✓	✓
LPDDR4		✓	✓	✓	✓	✓	✓	✓		Protocol controller, Memory controller	✓	✓	✓	✓
LPDDR4X				✓	✓		✓	✓	✓	Protocol controller, Memory controller	✓	✓	✓	✓
LPDDR3		✓	✓	✓	✓	✓				Protocol controller, Memory controller		✓	✓	
LPDDR2		✓								Protocol controller, Memory controller		✓	✓	
DDR5				✓	✓	✓	✓	✓	✓	Memory controller	✓	✓	✓	
DDR4		✓	✓	✓	✓	✓	✓	✓		Protocol controller, Memory controller		✓	✓	
DDR3	✓	✓	✓	✓	✓	✓				Protocol controller, Memory controller		✓	✓	
DDR2	✓									Protocol controller, Memory controller		✓	✓	

CXL	Process Technologies					Controllers	Configurations	IDE Security Module	Verification IP
	14/16nm	10nm	7nm	6nm	5nm				
CXL 3.x						Device, Host, Dual Mode, Switch Port	x4, x8, x16	✓	✓
CXL 2.0	✓	✓	✓	✓	✓	Device, Host, Dual Mode, Switch Port	x1, x2, x4, x8, x16	✓	✓

Interface IP							
CCIX	Process Technologies					Controllers	Verification IP
	14/16nm	12nm	7nm	6nm	5nm		
CCIX 1.1	✓	✓	✓	✓	✓	Endpoint, Root Port, Dual Mode, Switch	✓

USB	Processes												Controllers/Features	HS Access & Test	Verification IP
	55/ 65nm	40/ 45nm	28/ 22nm	20nm	14/ 16nm	12nm	10nm	7nm	6nm	5nm	4nm	3nm			
USB4						✓		✓	✓	✓		✓	Device Router, Host Router	✓	✓
USB-C 3.2 / DisplayPort 1.4 TX						✓		✓		✓	✓	✓	Host, Dual Role, DisplayPort TX, HDCP ESM, DSC	✓	✓
USB 3.2								✓	✓	✓	✓		Host, Device, Dual Role	✓	✓
USB-C 3.1 / DisplayPort 1.4					✓	✓	✓	✓	✓	✓			Host, Dual-Role, DisplayPort TX, HDCP ESM, DSC	✓	✓
USB-C 3.1					✓	✓		✓	✓	✓			Host, Device, Dual-Role	✓	✓
USB 3.1					✓	✓		✓	✓	✓	✓	✓	Host, Device, Dual-Role	✓	✓
USB-C 3.0			✓		✓	✓							Host, Device, Dual-Role	✓	✓
USB 3.0	✓	✓	✓	✓	✓	✓							Host, Device, Dual-Role	✓	✓
USB 2.0/USB-C 2.0	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓	Host, Device, Dual-Role	✓	✓
eUSB2										✓	✓	✓	Host, Device, Dual-Role	✓	✓

Interface IP

MIPI	Process Technologies									Controllers	Verification IP	Auto Grade
	40/45nm	28nm	22nm	20nm	14/16nm	12nm	7nm	6nm	3/4/5nm			
C/D-PHY					✓	✓	✓	✓	✓	CSI-2, DSI/DSI-2	✓	✓
D-PHY	✓	✓	✓	✓	✓	✓	✓	✓		CSI-2, DSI/DSI-2	✓	✓
M-PHY					✓	✓	✓	✓	✓	UFS, UniPro	✓	✓
CSI-2										Host, Device	✓	✓
DSI										Host, Device	✓	✓
DSC										Encoder, Decoder	✓	
DSI + DSC										DSI/DSI-2 + DSC Encoder	✓	
UniPro										v1.6, v1.8, v2.0	✓	
I3C										Multi-role, Target-Lite	✓	

Embedded Flash Storage	Process Technologies									Controllers	Verification IP	Inline Encryption	Auto Grade
	28nm	14/16nm	12nm	8nm	7nm	6nm	5nm	4nm	3nm				
UFS										✓	✓	✓	✓
UniPro										✓	✓		
M-PHY		✓	✓		✓	✓	✓	✓	✓	✓	✓		✓
eMMC	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
SD	✓	✓	✓		✓	✓	✓			✓	✓		
SDIO	✓	✓	✓		✓	✓	✓			✓	✓		

HDMI / DisplayPort	Process Technologies								Controllers	HDCP 2.3 Security Module	Verification IP
	40/45nm	28nm	14/16nm	12nm	7nm	5nm	4nm	3 nm			
HDMI 2.1			✓	✓	✓	✓	✓	✓	✓	✓	✓
HDMI 2.0	✓	✓	✓	✓					✓	✓	✓
DisplayPort 2.1								✓	✓	✓	✓
DisplayPort 1.4				✓	✓	✓	✓		✓	✓	✓

Interface IP			
Datapath IP	Synthesizable IP	Simulation Models (C++, Verilog)	Verification Models
Floating Point Functions	✓	✓	✓
Fixed Point Functions	✓	✓	✓
Trigonometric Functions	✓	✓	✓

AMBA	Synthesizable IP	Verification IP	Auto Grade
AMBA APB 3/4, AHB 2/5, AXI 3/4, ACE-Lite interconnect fabric, bridges, interconnect matrices and infrastructure IP	✓	✓	
AHB controller	✓	✓	
AXI DMA controllers	✓	✓	✓
SSI Controller (SPI/xSPI)	✓	✓	✓
I2C/SMBus Controller	✓	✓	
I2S/TDM Controller	✓	✓	
AMBA Advance peripherals (I^2C, I^2S, UART, SSI)	✓	✓	
Timers, WDT, RTC, interrupt controllers, GPIOs	✓	✓	

Foundation IP													
Embedded Memories	Process Technologies												
	65nm	55nm	40/ 45nm*	28nm	22nm*	14/ 16nm*	12nm*	10nm	8nm*	7/ 6nm*	5nm*	4nm	3nm
Ultra-High Density Single Port SRAM (UHD SP SRAM)					✓	✓	✓			✓	✓	✓	✓
Ultra-High Density Two Port SRAM (UHD 2P SRAM) / P2P SRAM				✓	✓	✓			✓	✓	✓	✓	✓
Ultra-High Density Two Port Register File (UHD 2P RF) / P2P RF	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Ultra-High Density One Port Register File (UHD 1P RF)					✓		✓			✓	✓	✓	✓
Ultra-High Speed Single Port SRAM (UHS SP SRAM)									✓			✓	
Ultra-High Speed Two Port Register File (UHS 2P RF)												✓	
High Speed Single Port SRAM (HS SP SRAM)	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
High Speed ROM (HS ROM)											✓		✓
High Speed Pseudo 4P/QP SRAM (HS P4P/QP SRAM)				✓		✓				✓			
High Speed Pseudo 2P SRAM (HS P2P SRAM)					✓								✓
High Speed Dual Port SRAM (HS DP SRAM)	✓	✓	✓	✓		✓	✓	✓	✓			✓	
High Speed Asynchronous Two Port Register File			✓	✓		✓							
High Speed Two Port Register File (HS 2P RF)					✓			✓	✓		✓		✓
High Speed One Port Register File (HS 1P RF) (Cache)	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
High Performance Core (HPC) Design Kit			✓	✓	✓	✓	✓		✓	✓	✓	✓	✓
High Density Single Port SRAM (HD SP SRAM)	✓	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓
High Density ROM (HD ROM)	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
High Density Dual Port SRAM (HD DP SRAM)	✓	✓	✓	✓	✓	✓	✓			✓	✓		✓
High Density Three Port Register File (HD 3P RF)											✓		
High Density 2P, 3P Async Latch Based Compiler				✓		✓				✓			
High Density Two Port Register File (HD 2P RF)	✓	✓	✓	✓	✓	✓	✓			✓	✓	✓	
High Density One Port Register File (HD 1P RF)	✓	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓
Extreme-High Density Two Port Register File (EHD 2P RF)											✓	✓	
Extreme-High Density One Port Register File (EHD 1P RF)											✓	✓	
Ternary Content-Addressable Memory (TCAM)	✓		✓	✓		✓		✓	✓	✓	✓	✓	✓
Multi-Port Memories										✓			
eMRAM					✓								

*Available in Consumer and Automotive

Foundation IP													
Logic Libraries	Process Technologies												
	65nm	55nm	40/45nm	28nm	22nm	14/16nm*	12nm*	8nm*	7nm*	6nm	5nm*	4nm	3nm
Ultra-Performance Library													✓
Ultra-Performance POK													✓
High-Speed Library	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓	✓	✓
High-Speed POK	✓	✓	✓	✓	✓	✓		✓	✓		✓	✓	✓
High-Density Library	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
High-Density POK	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
UHD Library	✓	✓	✓	✓	✓	✓		✓				✓	✓
UHD POK	✓	✓	✓	✓	✓	✓		✓				✓	✓
Extreme High Density (EHD) Library							✓						
EHD POK							✓						
Ultra-low leakage (thick oxide)			✓		✓	✓	✓						
High-Performance Core (HPC) Design Kit			✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

*Available in Consumer and Automotive

Non-Volatile Memory	Process Technologies											Bit Counts	Endurance (Write Cycles)
	150/ 180nm	110nm	130nm	80/ 90nm	55/ 65nm	40nm	28nm	22nm	16nm	12nm	5/6/ 7nm		
One-Time Programmable (OTP)	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	16 bit to 1 Mbit	1 per instance
Multi-Time Programmable (MTP) Medium-Density	180nm											16 bit to 512 Kbit	Up to 1,000
MTP EEPROM	180nm		✓		✓	✓						128 bit to 8 Kbit	Up to 1,000,000
MTP ULP	✓											64 bit to 4 Kbit	Up to 100,000
Few-Time Programmable (FTP) Trim	✓	✓	✓									64 bit to 4 Kbit	Up to 1,000
Auto Grade OTP			✓					✓				Up to 1 Mbit	1 per instance
Automotive AEC-Q100 Compliant OTP	✓				✓	✓	✓		✓			Up to 1 Mbit	1 per instance
Automotive AEC-Q100 Compliant MTP	✓		✓									128 bit to 8 Kbit (Up to 256Kb for Medium Density)	Up to 10,000

Foundation IP							
I/O Products	Process Technologies						
	22nm	14/16nm	12nm	6/7nm	5nm	4nm	3nm
General-purpose I/Os	✓	✓	✓	✓	✓	✓	✓
Specialty I/Os: I3C/I2C/LVDS/SDeMMC	✓	✓	✓	✓	✓	✓	✓
Auto Grade	✓			✓	✓		

Silicon Lifecycle Management (SLM) IP	Process Technologies									
In-Chip PVT Monitor IP	28nm	16nm	14nm	12nm	7nm	6nm	5nm	4nm	3nm	2nm
Process Detector	✓	✓		✓	✓*	✓	✓*	✓	✓	✓
Voltage Monitor	✓	✓		✓	✓*	✓	✓*	✓	✓	✓
Temperature Sensor	✓	✓	✓	✓	✓*	✓	✓*	✓	✓	✓
Digital Distributed Temperature Sensor									✓	✓
Distributed Temperature Sensor						✓	✓*	✓	✓	✓
Thermal Diode		✓		✓	✓	✓	✓*	✓	✓	✓
Catastrophic Temperature Sensor						✓	✓	✓	✓	✓
Glitch detector										✓
Soft IP										
PVT Controller	✓	✓		✓	✓*	✓	✓*	✓	✓	✓
Software Driver						✓	✓	✓	✓	✓
Other Monitor IP	In-Test					In-Field				
Path Margin Monitor Unit	✓					✓				
Path Margin Monitor Controller	✓					✓				
Clock & Delay Monitor	✓					✓				

IP Test Automation	Embedded Memories	Non-Volatile Memories	Speciality Memories	DRAM Memory	Interface IP Test	PVT Monitor IP Test
Hierarchical test for multiple IP cores					✓*	✓*
Memory test, repair and diagnostics	✓*	✓	✓*	✓		

* Automotive Grade

Security IP				
Security	Synthesizable IP	Software	Safety Compliant	Verification IP
Cryptography IP	✓	✓	✓	
Physical Unclonable Function (PUF)	✓	✓	✓	
Security Protocol Accelerators	✓	✓	✓	
Hardware Secure Modules with Root of Trust	✓	✓	✓	
HDMI/DisplayPort/USB Type C Content Protection (HDCP 2.3)	✓	✓		✓
PCIe & CXL Integrity and Data Encryption (IDE)	✓	✓	✓	✓
DDR/LPDDR Inline Memory Encryption (IME)	✓	✓		✓
Ethernet Media Access Control Security (MACsec)	✓	✓		✓

Accelerate Development of Performance-Efficient SoCs

Synopsys' ARC® Processor IP is a portfolio of CPUs, DSPs and NPUs that SoC designers can optimize for a wide range of uses, from deeply embedded to high-performance host applications, in a variety of market segments. The portfolio includes 32- and 64-bit ARC-V™ Processor IP based on the open-standard RISC-V ISA.

ARC processors offer a high degree of configurability that enables designers to tailor each processor instance to meet their specific performance, power and area requirements. ARC processors are also extensible, allowing designers to customize their implementation with proprietary instructions or logic that can dramatically improve performance and reduce energy consumption.

All Synopsys ARC processors are synthesizable and can be implemented in any foundry or process technology.

Synopsys ARC processors are supported by a broad ecosystem of commercial and open source tools, operating systems and middleware. This includes a full set of software development tools from Synopsys, offerings from leading industry vendors who are members of the ARC Access Program, and a broad suite of free and open source software available through embARC.org.

Processor IP											
ARC-V (RISC-V) 64-bit Processors	Multicore Support	L1 Cache (I & D)	L2 Cache (unified, per core)	L3 Cache (shared)	MMU	Hardware Virtualization	Floating Point	Real-time Trace Support	Vector Extensions (RVV)	Safety Compliant (ISO 26262)	Cybersecurity Compliant (ISO 21434)
RPX-100/100V		Up to 64K	Up to 1M	Up to 16M	✓	✓	H, S, D	Opt	✓ (100V only)		✓
RPX-105/105V	Up to 16	Up to 64K	Up to 1M	Up to 16M	✓	✓	H, S, D	Opt	✓ (105V only)		✓
RPX-110-FS/110V-FS		Up to 64K	Up to 1M	Up to 16M	✓	✓	H, S, D	Opt	✓ (110V only)	✓	✓
RPX-115-FS/115V-FS	Up to 16	Up to 64K	Up to 1M	Up to 16M	✓	✓	H, S, D	Opt	✓ (115V only)	✓	✓

ARC-V (RISC-V) 32-bit Processors	Multicore Support	CCM (I & D)	L1 Cache (I & D)	L2 Cache (shared)	MMU	Hardware Virtualization	Floating Point	Real-time Trace Support	DSP Extensions	Vector Extensions (RVV)	Safety Compliant (ISO 26262)	Cybersecurity Compliant (ISO 21434)
RHX-100/100V		Up to 16M	Up to 64K	Up to 16M	Opt	✓	H, S, D	Opt		✓ (100V only)		✓
RHX-105/105V	Up to 16	Up to 16M	Up to 64K	Up to 16M	Opt	✓	H, S, D	Opt		✓ (105V only)		✓
RHX-110-FS/110V-FS		Up to 16M	Up to 64K	Up to 16M	Opt	✓	H, S, D	Opt		✓ (110V only)	✓	✓
RHX-115-FS/115V-FS	Up to 16	Up to 16M	Up to 64K	Up to 16M	Opt	✓	H, S, D	Opt		✓ (115V only)	✓	✓
RMX-100/100D		Up to 2M	Up to 64K (I only)				Opt (S, D)	Opt	✓ (100D only)	✓ (100D only)		✓
RMX-500/500D		Up to 2M	Up to 64K				Opt (S, D)	Opt	✓ (500D only)	✓ (500D only)		✓
RMX-110-FS		Up to 2M	Up to 64K (I only)				Opt (S, D)	Opt	✓		✓	✓
RMX-510-FS		Up to 2M	Up to 64K				Opt (S, D)	Opt	✓		✓	✓

Processor IP								
ARC (Classic) 64-bit Processors	**Multicore Support**	**CCM (I & D)**	**L1 Cache (I & D)**	**L2 Cache**	**MPU**	**MMU**	**Floating Point (SIMD)**	**Trace**
HS66, HS66MP	Up to 12 (MP)	Up to 16M	Up to 64K	Up to 64M	Opt	Opt	Opt	Opt
HS68, HS68MP	Up to 12 (MP)	Up to 16M	Up to 64K	Up to 64M	Opt	✓	Opt	Opt

ARC (Classic) 32-bit Processors	**Multicore Support**	**CCM (I & D)**	**L1 Cache (I & D)**	**L2 Cache**	**MPU**	**MMU**	**DSP**	**Floating Point**	**Safety Compliant (ISO 26262)**	**Side Channel Protection**
HS58, HS58MP	Up to 12	Up to 16M	Up to 64K	Up to 64M	Opt	✓		Opt		
HS57D, HS57DMP	Up to 12	Up to 16M	Up to 64K	Up to 64M	Opt	Opt	✓	Opt		
HS56, HS56MP	Up to 12	Up to 16M	Up to 64K	Up to 64M	Opt	Opt		Opt		
HS48FS, HS48FSx4	Up to 4	Up to 16M	Up to 64K	Up to 8M	Opt	✓		Opt	✓	
HS47DFS, HS47DFSx4	Up to 4	Up to 16M	Up to 64K		Opt	Opt	✓	Opt	✓	
HS46FS, HS46FSx4	Up to 4	Up to 16M	Up to 64K		Opt	Opt		Opt	✓	
HS47D, HS47Dx2, HS47Dx4	Up to 4	Up to 16M	Up to 64K		Opt	Opt	✓	Opt		
HS45D, HS45Dx2, HS45Dx4	Up to 4	Up to 16M			Opt		✓	Opt		
HS48, HS48x2, HS48x4	Up to 4	Up to 16M	Up to 64K	Up to 8M		✓		Opt		
HS46, HS46x2, HS46x4	Up to 4	Up to 16M	Up to 64K		Opt	Opt		Opt		
HS44, HS44x2, HS44x4	Up to 4	Up to 16M			Opt			Opt		
HS38, HS38x2, HS38x4	Up to 4	Up to 16M	Up to 64K	Up to 8M		✓		Opt		
HS36, HS36x2, HS36x4	Up to 4	Up to 16M	Up to 64K		Opt	Opt		Opt		
HS34, HS34x2, HS34x4	Up to 4	Up to 16M			Opt			Opt		
EM11D/9D		Up to 2M	Up to 64K (11D)		Opt		✓	Opt		
EM7D/5D		Up to 2M	Up to 64K (7D)		Opt		✓	Opt		
EM6/4		Up to 2M	Up to 64K (6)		Opt			Opt		
EM22FS		Up to 2M	Up to 64K		Opt		✓	Opt	✓	
SEM110/120D		Up to 2M			Opt		✓ (120D only)	Opt		✓
SEM130FS		Up to 2M			Opt		✓	Opt	✓	✓

Processor IP				
ARC Processor IP Subsystems	**Supported ARC Processors**	**Hardware Accelerators**	**Integrated Peripherals**	**Included Software**
IoT Communications IP Subsystem	EM11D	✓	SPI, UART(s), GPIO, Digital Front End (DFE), PMU, USIM, MIPI RFFE and RTC	DSP library, base communications library, device drivers
Data Fusion IP Subsystem	EM5D, EM7D, EM9D, EM11D	✓	SPI, I²C, I²S, UART, PDM, ADC I/F, APB I/F, GPIO	DSP library, audio processing library, peripheral I/O drivers (bare metal), reference designs
Sensor and Control IP Subsystem	EM4, EM6	✓	SPI, I²C, PWM, UART, ADC I/F, DAC I/F, APB I/F, GPIO	DSP library, motor control library, peripheral I/O drivers (bare metal), reference designs

ARC VPX DSP Processors	Multicore configurations	Vector Execution Units/VLIW	Vector Length	Vector Floating Point Unit	Vector Math Accelerator (configuration option)	Safety Compliant (ISO 26262)
VPX2/VPX2FS	1, 2	3	128-bit	Opt	✓	✓ (FS only)
VPX3/VPX3FS	1, 2	3	256-bit	Opt	✓	✓ (FS only)
VPX5/VPX5FS	1, 2, 4	3	512-bit	Opt	✓	✓ (FS only)

ARC NPX Neural Processors	MACs	L2 Shared Memory	Tensor Accelerator	Tensor Floating Point Unit	Memory Management Unit (MMU)	Virtualization Support	Safety Compliant (ISO 26262)
NPX6-1K/NPX6-1KFS	1,024	0-64 MB	✓	Opt	✓	✓	✓ (FS only)
NPX6-4K/NPX6-4KFS	4,096	0-64 MB	✓	Opt	✓	✓	✓ (FS only)
NPX6-8K/NPX6-8KFS	8,192	0-64 MB	✓	Opt	✓	✓	✓ (FS only)
NPX6-12K/NPX6-12KFS	12,288	0-64 MB	✓	Opt	✓	✓	✓ (FS only)
NPX6-16K/NPX6-16KFS	16,384	0-64 MB	✓	Opt	✓	✓	✓ (FS only)
NPX6-24K/NPX6-24KFS	24,576	0-64 MB	✓	Opt	✓	✓	✓ (FS only)
NPX6-32K/NPX6-32KFS	32,768	0-64 MB	✓	Opt	✓	✓	✓ (FS only)
NPX6-48K/NPX-48KFS	49,152	0-64 MB	✓	Opt	✓	✓	✓ (FS only)
NPX6-64K/NPX6-64KFS	65,536	0-64 MB	✓	Opt	✓	✓	✓ (FS only)
NPX6-96K/NPX6-96KFS	98,304	0-64 MB	✓	Opt	✓	✓	✓ (FS only)

Embedded Vision Processors	Vision CPU MACs	DNN/CNN Accelerator MACs (non-FuSa option)	# of Scalar Cores	# of Vector DSPs	Vector DSP Bit Width	L1 Cache Coherency	Scalar Floating Point Unit	Vector Floating Point Unit	Safety Compliant (ISO 26262)
EV71/EV71FS	64	880, 1760, or 3520	1	1	512		✓	Opt	✓ (FS only)
EV72/EV72FS	128	880, 1760, or 3520	2	2	512	✓	✓	Opt	✓ (FS only)
EV74/EV74FS	256	880, 1760, or 3520	4	4	512	✓	✓	Opt	✓ (FS only)

IP Accelerated Initiative

With IP Accelerated, Synopsys has augmented its broad portfolio of silicon-proven Synopsys IP with SoC architecture design support, IP subsystems, signal integrity/power integrity analysis and IP hardening, and comprehensive silicon bring-up support to accelerate your product development cycle.

IP Subsystems support many protocols and deliveribles for IP integration including configuration scripts, test environment, test scripts, linting, CDC checks, RDC checks, synthesis scripts and implementation scripts. The subsystems also include AMBA or native bus, clock management, reset, DMA, interrupts, memory, power management, debug and test logic.

Hardening and SIPI provide a GDSII for integration in an SoC and include On-chip decoupling capacitance, power and ground pins, PHY & SDRAM termination strategy, SoC package design, PCB stack-up and trace width/spacing, performance at required data rate, read/write/address, and command/control timing budgets.

With your vision and our expertise, we can tune our IP to your SoC, enabling your team to focus on product differentiation.

IP Subsystems				
Interface IP Subsystems	**Supported IP**	**Multi-Protocol Support**	**Integrated Logic**	**Included Scripts**
IP Protocol-Specific Subsystems	USB, PCIe, DDR, HBM, UCIe, Ethernet, MIPI, AMBA, Security, MACsec, PCIe switch, CXL 2.0 switch	✓	AMBA or native bus, clock management, reset, DMA, interrupts, memory, power management, debug and test logic	Configuration scripts, test environment, test scripts, linting, CDC checks, RDC checks, synthesis scripts, implementation scripts

Interface IP Subsystems	**Combo Subsystems**	**Auto Grade**	**UVM**	**Spyglass**	**SRAM/MBIST**	**UPF**	**DFT**
PCIe/CXL	PCIe-Ethernet, PCIe-USB, PCIe-SATA PCIe-CCIX, CXL	ASIL B	✓	✓	✓	✓	✓
DDR3/4/5	DDR4/5, LPDDR4/4X/5/5X						
HBM3							
UCIe							
Ethernet	Ethernet-PCIe, Ethernet-USB						
USB	USB-DP, USB-DP-HDMI, USB-PCIe, USB-Ethernet, eUSB						
MIPI	CSI, DSI, UFS						

Configurable IP Subsystems	**Combo Subsystems**	**Auto Grade**	**UVM**	**Spyglass**	**SRAM/MBIST**	**UPF**	**DFT**
CXL 2.0 switch	✓	ASIL B	✓	✓	✓	✓	✓
PCIe switch							
MACsec							

IP Hardening											
Supported IP	Multi-protocol Support	Synthesis to GDSII	Floor Planning	Scan Insertion	Power Grid	Skew Balancing	RDL Routing	Bump Assignment	IR/EM-Analysis	DRC/LVS	GLS
DDR/LPDDR	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
HBM2E / HBM3											
UCIe											
PCIe											

Signal/Power Integrity Analysis										
Supported IP	Multi-protocol Support	Floorplan Review	Pre/Post Layout Analysis	Decap Cell Size/Placement	Power Impedance Simulations	Eye Quality Analysis	End to End Analysis	Timing Budget Analysis	Signal Quality PVT Corner Analysis	Full Report
DDR/LPDDR	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
HBM2E / HBM3										
UCIe										
HBI										
PCIe										
MIPI										
Ethernet										

For more information on Synopsys IP, visit synopsys.com/ip.

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